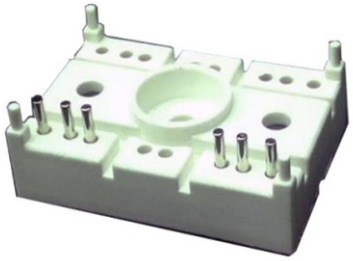
Anti-parallel Thyristor Module, 100A
(Low Profile Package)

FEATURES

- High voltage
- 3000V_{RMS} isolating voltage
- High surge capability
- **Planar SCR chips**
- Heat transfer and isolation through direct copper bonded aluminum oxide ceramic (Al_2O_3 DBC)
- Simple mounting (One screw mounting)
- Compliant to RoHS
- Designed and qualified for multiple level

RoHS COMPLIANT

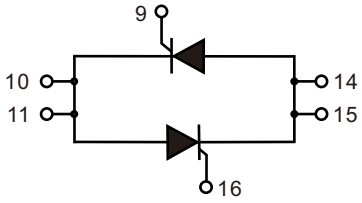


Low profile package

APPLICATIONS

- Soft starters
- Battery charges
- Light control
- Power converters
- Heat and temperature control

"**KQ**" Circuit Configuration :



PRODUCT SUMMARY	
$I_{T(RMS)}$	100A

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNIT
$I_{T(RMS)}$	85°C	100	A
I_{TSM}/I_{FSM}	50 Hz	1500	
	60 Hz	1576	
I^2t	50 Hz	11.25	kA^2s
	60 Hz	10.31	
$I^2\sqrt{t}$		112.5	$kA^2\sqrt{s}$
V_{DRM}/V_{RRM}	Range	800 to 1600	V
T_J	Range	-40 to 150	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	VOLTAGE CODE	V_{RRM}/V_{DRM}, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	V_{RSM}/V_{DSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	I_{RRM}/I_{DRM} AT 125°C mA
NK100KQ	08	800	900	15
	12	1200	1300	
	16	1600	1700	

FORWARD CONDUCTION						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**VALUES**	**UNIT**
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction, half sine wave, 50Hz, T_C = 85°C			100	A
Maximum peak, one-cycle , on-state non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sine half wave, initial T_J = T_J maximum	1500	A
		t = 8.3ms			1576	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied	Sine half wave, initial T_J = T_J maximum	11.25	kA^2s
		t = 8.3ms			10.31	
		t = 10ms	100%V_{RRM} reapplied		7.8	
		t = 8.3ms	100%V_{RRM} reapplied		7.2	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			112.5	$kA^2\sqrt{s}$
Maximum on-state voltage drop	V_{TM}	I_{TM} = 200A, T_J = 25°C, 180° conduction			1.8	V
Maximum holding current	I_H	Anode supply = 6V, resistive load, T_J = 25°C			150	mA
Maximum latching current	I_L				400	

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum peak reverse and off-state leakage current	I_{RRM} I_{DRM}	T_J = 125°C	15	mA
RMS isolation Voltage	V_{ISO}	50 Hz, circuit to base, all terminals shorted	2500 (1 min) 3000 (1 s)	V
Critical rate of rise of off-state voltage	dV/dt	T_J = T_J maximum, exponential to 67% rated V_{DRM}	1000	V/μs

TRIGGERING					
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**VALUES**	**UNIT**
Maximum peak gate power	P_{GM}	t_p ≤ 5 ms, T_J = T_J maximum		10	W
Maximum average gate power	$P_{G(AV)}$	f = 50 Hz, T_J = T_J maximum		3	W
Maximum peak gate current	I_{GM}	t_p ≤ 5 ms, T_J = T_J maximum		3	A
Maximum peak negative gate voltage	$-V_{GT}$	t_p ≤ 5 ms, T_J = T_J maximum		10	V
Maximum required DC gate voltage to trigger	V_{GT}	T_J = 25°C	Anode supply = 6V, resistive load; R_a = 1Ω	0.7 to 1.5	V
Maximum required DC gate current to trigger	I_{GT}	T_J = 25°C	Anode supply = 6V, resistive load; R_a = 1Ω	20 to 100	mA
Maximum gate voltage that will not trigger	V_{GD}	T_J = T_J maximum, 66.7% V_{DRM} = applied		0.25	V
Maximum gate current that will not trigger	I_{GD}	T_J = T_J maximum, 66.7% V_{DRM} = applied		10	mA
Maximum rate of rise of turned-on current	dI/dt	T_J = 25°C, I_{GM} = 1.5A, t_r ≤0.5 μs		150	A/μs

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum junction operating temperature range	T_J		-40 to 150	°C
Maximum storage temperature range	T_{stg}		-40 to 150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.6	°C/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface, smooth, flat and greased	0.18	
Mounting torque, ±10% module to heatsink, M4		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	2	N·m
Approximate weight			22	g
			0.78	oz.
Case style			Low Profile package (Nell-Top 2)	

Ordering Information Table

Device code

NK	100	KQ	12
①	②	③	④

1 - Nell's Low profile module (Nell-Top 2)
2 - Current rating : $I_{T(RMS)}$
3 - Circuit configuration type
4 - Voltage code x 100 = V_{DRM}/V_{RRM}

Fig.1 On-state Voltage characteristics (per thyristor)

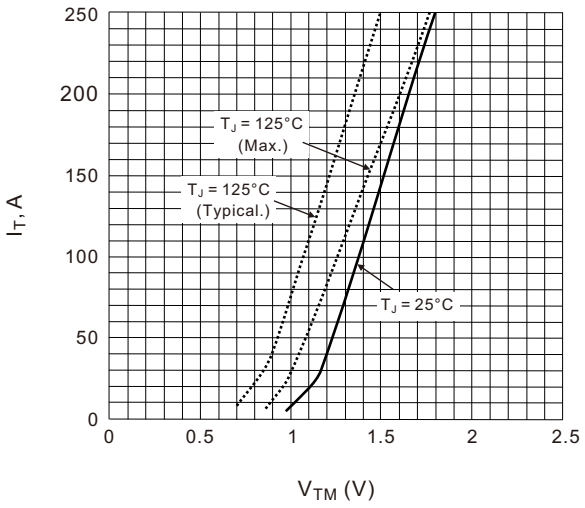


Fig.2 Transient thermal Impedance vs. time (per thyristor)

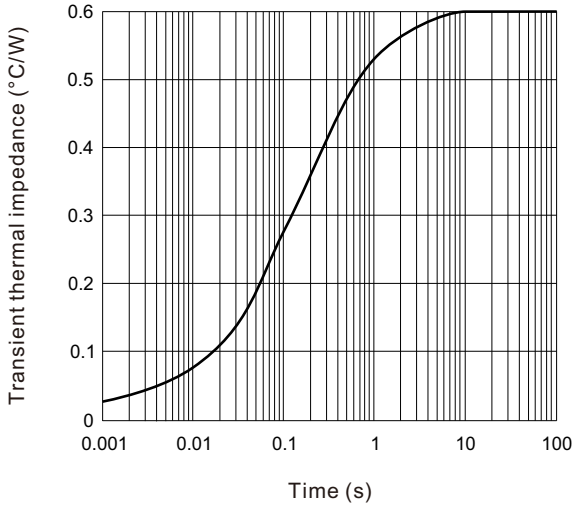


Fig.3 Power Dissipation Vs. RMS Current

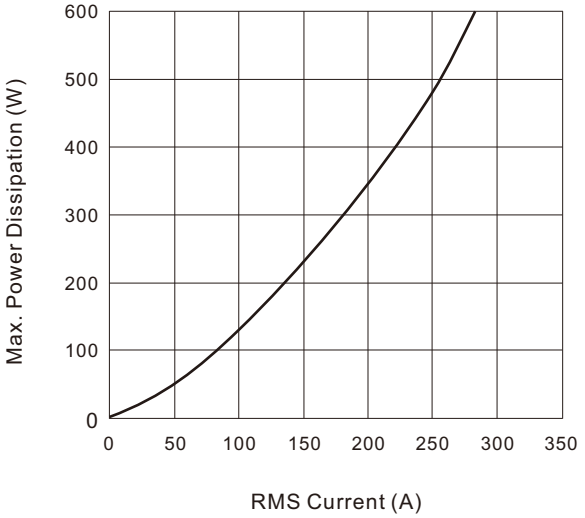


Fig.4 Surge On-state Current Vs. Cycles

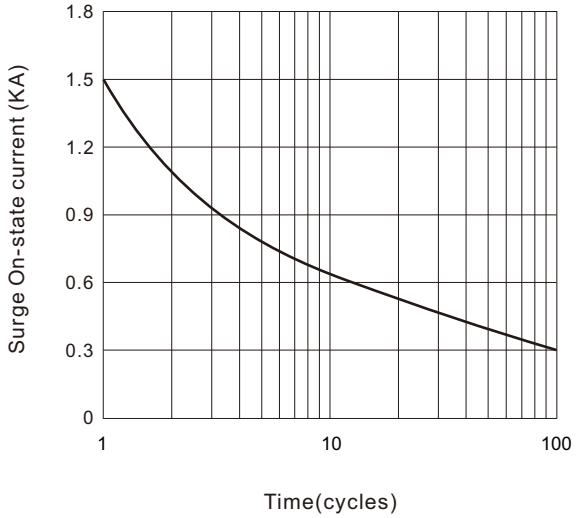
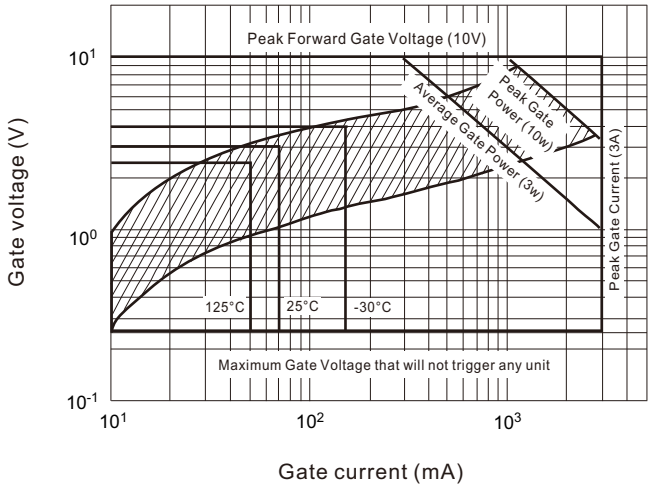
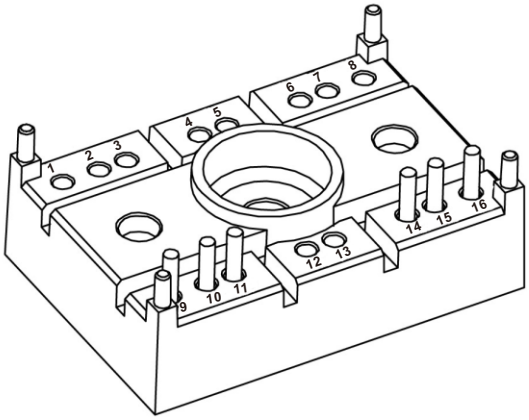
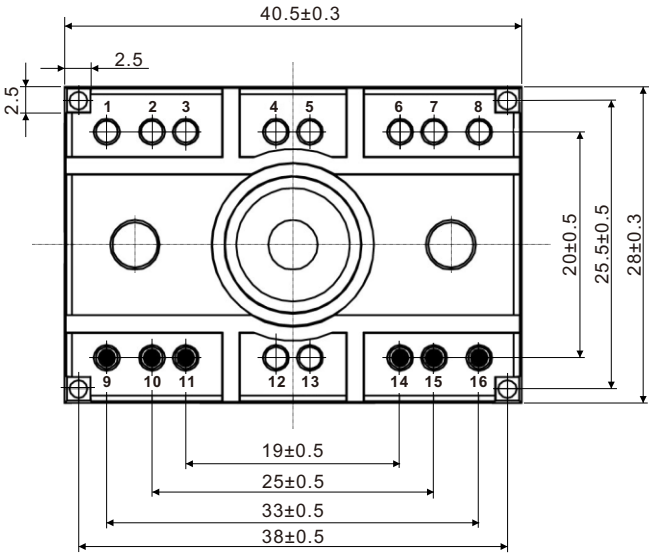
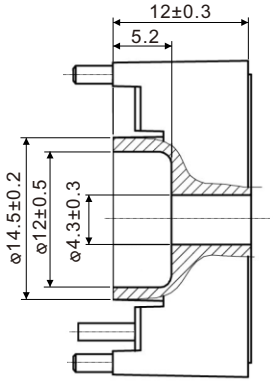


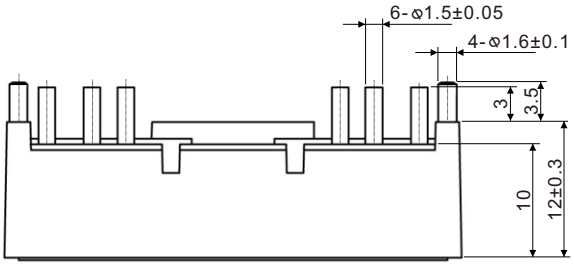
Fig.5 Gate characteristics



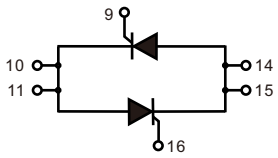








"**KQ**" Circuit Configuration :



All dimensions in millimeters(inches)